Test Report V1.0
SEE Test Plan for Boeing Rad-Hard By Design Shift Register Test Structures

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Test Date(s): June 16, 2005 Report Date: January 11, 2006

I. Introduction

This study is being undertaken to determine the Linear Energy Transfer (LET) threshold (LET_{th}) and LET characterization of the transient/upset susceptibility for the shift register (SR) test structures designed by Boeing and partners under the DARPA Rad-Hard By Design (RHBD) Program; single event latchup (SEL) will be monitored for, but no specific SEL test is planned. The device under test (DUT) will be monitored for errors in the output of the shift register strings and for destructive events (current increases) induced by exposing it to a heavy ion beam at the Brookhaven National Laboratories' Single Event Upset Test Facility (SEUTF).

II. Devices Tested

One sample was tested with device markings on lid of MOSIS T51R-AJ. The device is designed by Boeing, et al and manufactured at IBM via the DoD's Trusted Foundry Program and was characterized prior to exposure. The device has no lot date code but is a test chip delivered from IBM in June of 2005.

The device technology is 0.13μm CMOS bulk. The device is packaged in a 280-pin pin grid array (PGA) package. The device was packaged and bonded for test by MOSIS (NO thinning, plasma etching, delivered with lid not attached. i.e. no special prep). The overlayer thicknesses for LET calculation are 2.5 microns Al (interconnect or fill), 0.55 Cu (interconnect or fill), 4.7 microns isolation oxide, 0.45 microns nitride, and 2.5 micron polyimide.

Three shift register blocks (A, B, and C) totaling seventeen shift registers will be tested. These seventeen shift registers were tested for upsets by clocking a known pattern to the inputs and verifying that the same pattern emerges at the outputs. Each SR string is 1920 stages or bits. Outputs from as many as seven separate SR strings were simultaneously monitored during test.

A more detailed description of the shift register test group is given in appendix 1.

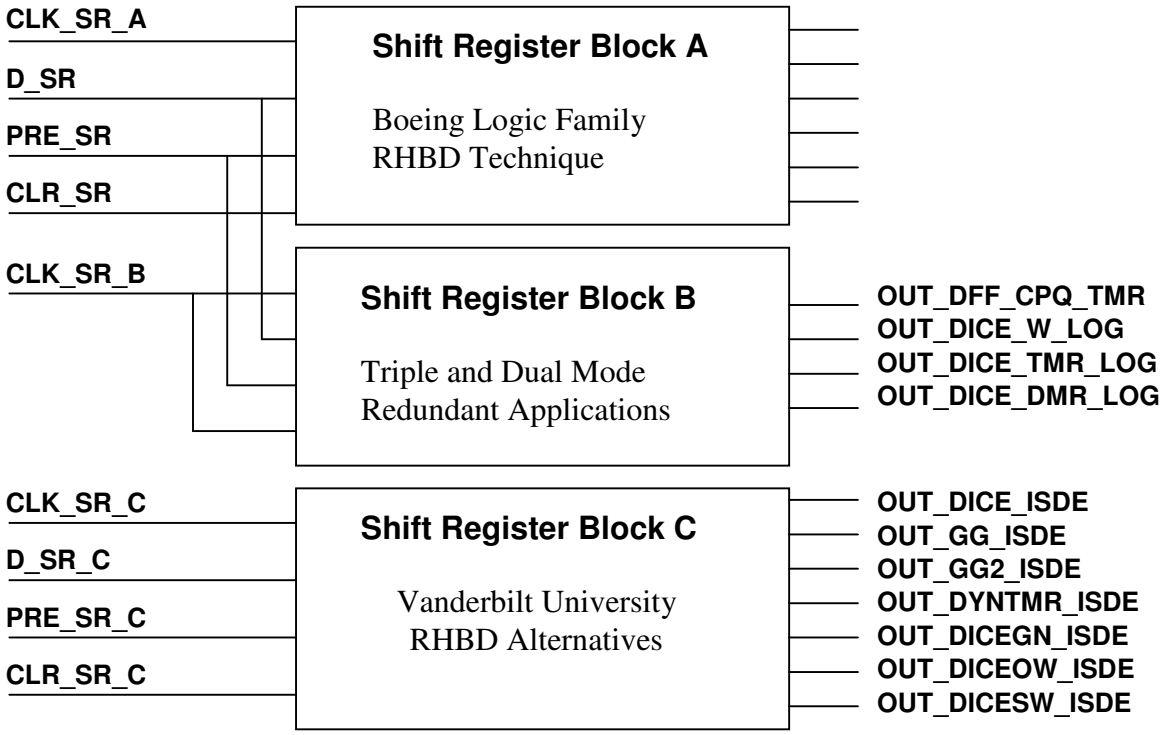


Figure 1. Shift Register Block Organization.

III. Test Facility

Facility: Brookhaven National Laboratories' (BNL) Single Event Upset Test Facility (SEUTF)
Flux: ~1 x 10^3 to 1 x 10^5 particles/cm^2/s
Fluence: All tests were run to 1 x 10^7 p/cm^2, until destructive or functional events occurred, or until 100 or more SEUs have occurred.

Ions used are listed in the table below. Determining the variances by SR design of LET_{th} and associated curves are the prime objective.

Ion	Incident LET (MeV•cm^2/mg)	Energy in MeV	Range in um (Si)
C-6	1.46	99.6	180.43
Si-14	7.81	187	77.16
Cl-17	11.5	212	64.41
Ti-22	19.6	232	47.8
Ni-28	27.9	270	44.56

Additional LETs will be obtained by varying the angle of incidence and calculating effective LET and fluence levels.

Figure 2. Picture of SEUTF Vacuum Test Chamber

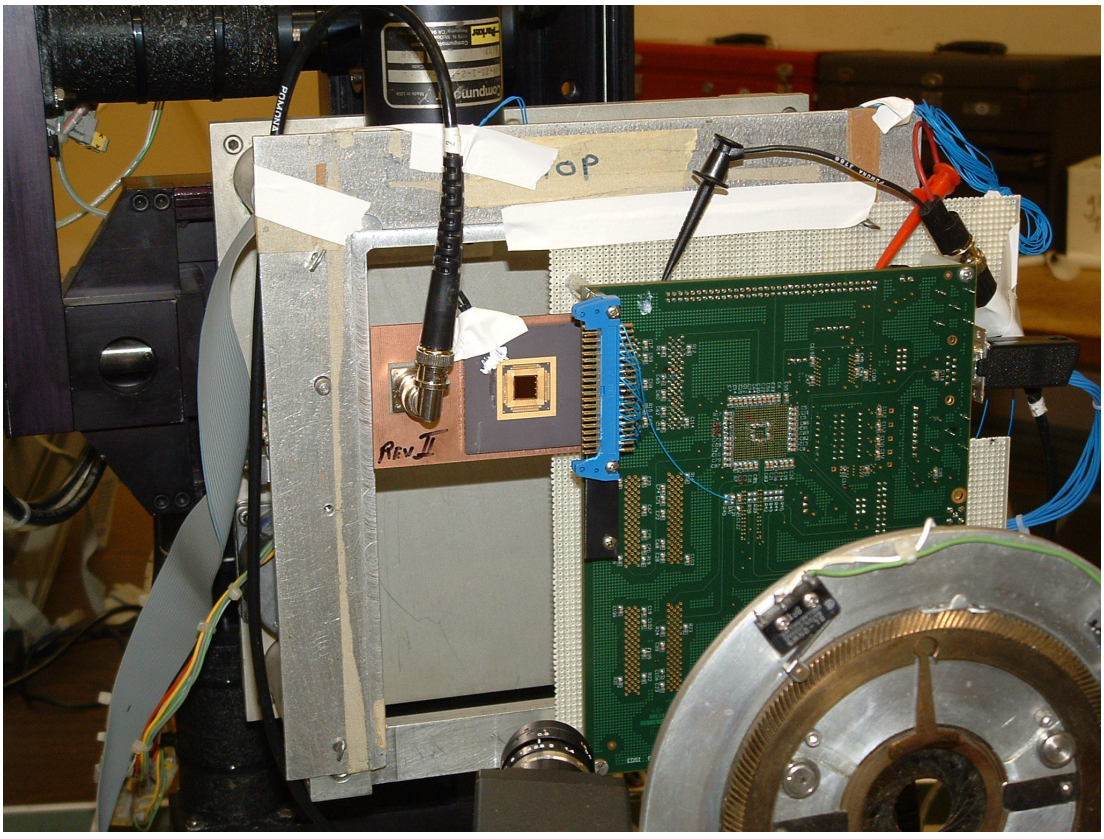


Figure 3. Test Set and DUT at BNL

IV. Test Conditions and Error Modes

Test Temperature: SEU testing was performed at nominal room temperature (30C); no high-temp SEL was performed. A thermoelectric cooler (TEC) will be utilized to maintain nominal room temperature while operating in the SEUTF vacuum chamber.

Test Patterns: Four test patterns will be used: all 1's, all 0's, 0101, and 0011. If time allows for test development, a PRN (2^N-1) will also be used.

Power Supply and IO Voltage: Testing will be at 1.2V.

Parameters of Interest: Power supply current was monitored looking for anomalous conditions such as SEL. Current operating consumption will be a function of shift register blocks and operating speed.

Test Note: Only one SR block (A, B, or C) will operate at a time due to power considerations.

SEE Conditions: Errors will be defined as a mismatch between input (or expected) test pattern and output pattern for each SR string. Errors may be single, double, or multiple consecutive bits. Data collection will be N events of X type per SR string (normalization per stage will be done post-irradiation) Functional interrupts are not expected on the SR strings. Power supply current will be monitored.

V. Test Methods

1. Test hardware configuration (Hak Kim)
    a. Include block diagrams of test setup
    b. Schematics of daughterboard and connector pinouts
    c. Connector type
    d. Thermal control/measurement
    e. DUT pinout and connection to test setup
    f. Power control
2. Test control/operations (Melanie Berg)
    a. Top-level description of VHDL control of DUT.
    b. Description of error detection.
    c. Description of data collection, storage, (real-time error counting?)

VI. Test Performance

The following individuals were on-site at the SEUTF during the test:

- Ken LaBel/NASA/GSFC
- Hak Kim/MEI
- Melanie Berg/MEI

One device was mounted on a separate daughtercard. The DUT was mounted and checked with the test system, placed into the vacuum chamber, then evacuated, and re-checked prior to initial irradiation.

In general each test run was as follows:

- Power on and initialize test system
- Select SR block, test frequency, power supply and I/O voltage, etc for test
- Power on DUT
- Begin I/O to DUT
- Verify no errors are occurring (may perform run with beam at blank spot and not on DUT)
- Begin irradiation and count errors
- Stop irradiation at fixed fluence level, anomalous condition, or statistically significant number of events. SEL occurrence should send halt signal automatically to BNL control computer to close irradiation shutter.
- If errors are occurring after the beam is stopped, halt I/O (may require DUT power cycle). Else
- If other anomalous conditions have occurred (such as SEL), then halt I/O, record anomaly (power supply current trace)
- If no anomalous conditions have occurred, the next run may start with Begin I/O. Else
- Power cycle DUT, etc…

The test matrix will work from the following parameter space for capture by EXCEL spreadsheet:

- Run number
- DUT #
- DUT identification
- SR Block (A, B, or C)
- Vdd, I/O Voltage (1.2V)
- Test Pattern (1, 0, 01, 0011)
- Test Frequency (1-100 MHz)
- Ion (C to I)
- Ion Energy
- Range in um (Si)
- Angle of Incidence (TBD pending test fixture limitation)
- Effective LET (surface)
- Effective LET (through overlayers)
- Effective Flux
- Effective Fluence
- Error types per SR string (single, double, etc)
- Measured error type cross-section in cm^2 per SR string (N errors per error type divided by effective fluence)

The expected test matrix exceeds the beam time allotted (nominal 8 hours, possible up to 12) and may be pared down using some initial test runs at low/high operating speeds at a nominal LET such as 11.5 (unhardened should upset, but hardened should not).

VII. Test Configuration

Test Parameters:

- Vdd = 1.2V
- Frequency = 12.5 MHz
- Test Patterns (A): 0101 (chk-01), all-1, No testing of all-0 on Block A was possible due to a discovered bug in VHDL tester code.
- Test Patterns (B): 0101 (chk-01), all-1, all-0 (pattern 0011 was not used, tester VDHL was not verified prior to test)
- Temp = 30C
- LET_{th} is highest LET at which 0 errors were seen at a fluence of 1E7 p/cm^2
- Sigma measured have ~50% error bars and are on a per stage (i.e., N errors/(fluence*1920 SR per string)

One sample was tested with device markings on lid of MOSIS T51R-AJ.

No testing was performed on Block C due to a VHDL tester code issue w/ a known non-function SR string. (We did not have proper development software to make the change and the error rate on the bad SR string overwhelmed our buffers.)

VIII. Test Results

Test results are summarized in tables and graphs below. ~ 100 krad(Si) was accumulated on the device under test (DUT) with no apparent functional or parametric degradation.

Block A results:

Shift register string	**LET_{th}**	**Sigma per SR at max LET (33.2) for single errors in cm^2**	**Notes**
SR_DFF_CPQ_soft	~1.5	1.79E-7	Burst errors at observed at LET = 21.45
SR_DFF_CPQ_hard	1.72<LET_{th}<8.49	1.29E-7	Burst errors at observed at LET = 21.45
SR_DICE_soft	21.45<LET_{th}<28.44	1.51E-8	Burst errors at observed at LET = 28.44
SR_DICE_soft_wide	21.45<LET_{th}<28.44	1.51E-8	Burst errors at observed at LET = 28.44
SR_DICE_mdm	14.69<LET_{th}<21.45	2.18E-8	Burst errors at observed at LET = 28.44
SR_DICE_hard	14.69<LET_{th}<21.45	2.47E-8	Burst errors at observed at LET = 28.44

Burst errors details will be available in a few weeks.

Block B results:

Shift register string	LET_{th}	Sigma per SR at max LET (33.2) for single errors in cm^2	Notes
SR_DF_CRQ_tmr	$8.49<LET_{th}<12.57$	4.83E-8	Burst errors at observed at LET = 8.49
SR_DICE_w_logic	$8.49<LET_{th}<12.57$	1.61E-8	Burst errors at observed at LET = 8.49
SR_DICE_TMR_LOG	$14.69<LET_{th}<21.45$	2.84E-8	Burst errors at observed at LET = 28.44
SR_DICE_DMR_LOG	$14.69<LET_{th}<21.45$	2.88E-8	Burst errors at observed at LET = 28.44

Burst errors details will be available in a few weeks. May have seen one event at LET < 2.

Other: two anomalous runs occurred where Idd dropped from operating Idd (17-24 mA) to 2-2.4 mA. Condition cleared with a power cycle.

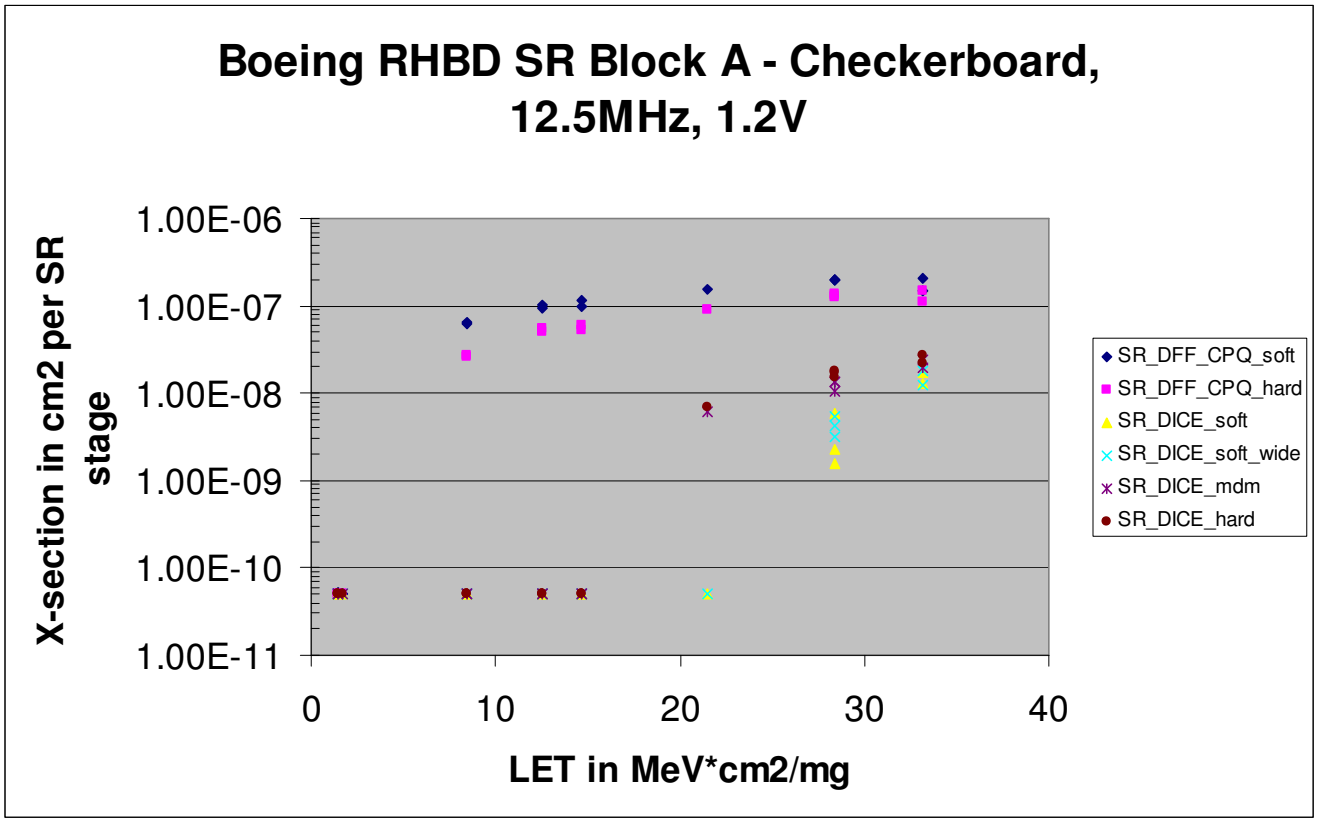


Figure 4. Cross section vs LET for the Boeing RHBD SR Block A.

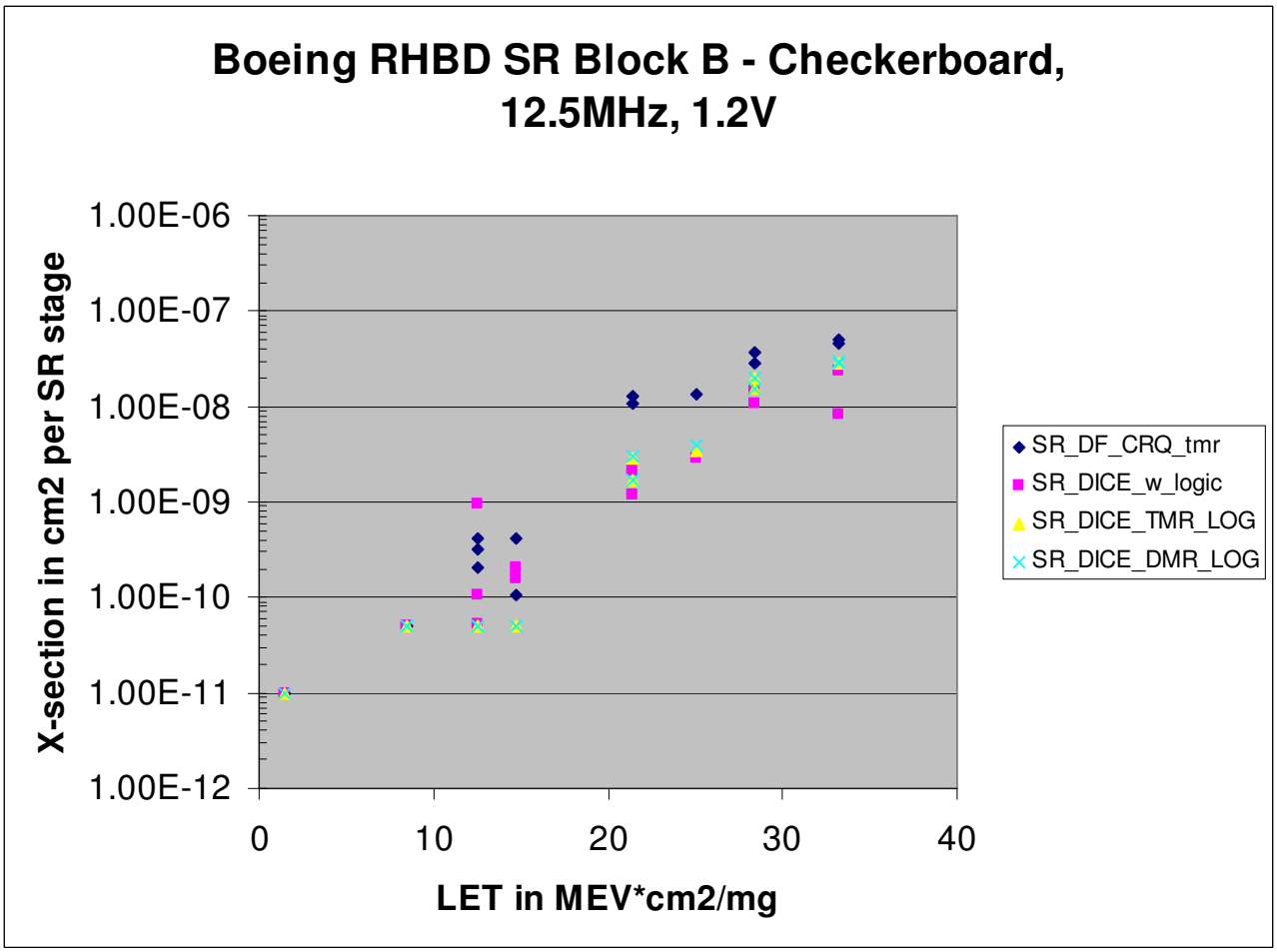


Figure 5. Cross section vs LET for the Boeing RHBD SR Block B.

Limited tests were done on static all-1 and all-0 patterns.

No data collection was possible of all-0 on Block A due to a discovered bug in VHDL tester code, however, we did observe errors occurring on Block A during debug operations under irradiation (how we discovered the problem) at LET of 12.57.

No errors were observed with the all-1 pattern on Block A to highest tested LET of 33.2 on all SR strings except SR_DFF_CPQ_soft which observed SEUs at lowest tested LET of 12.57.

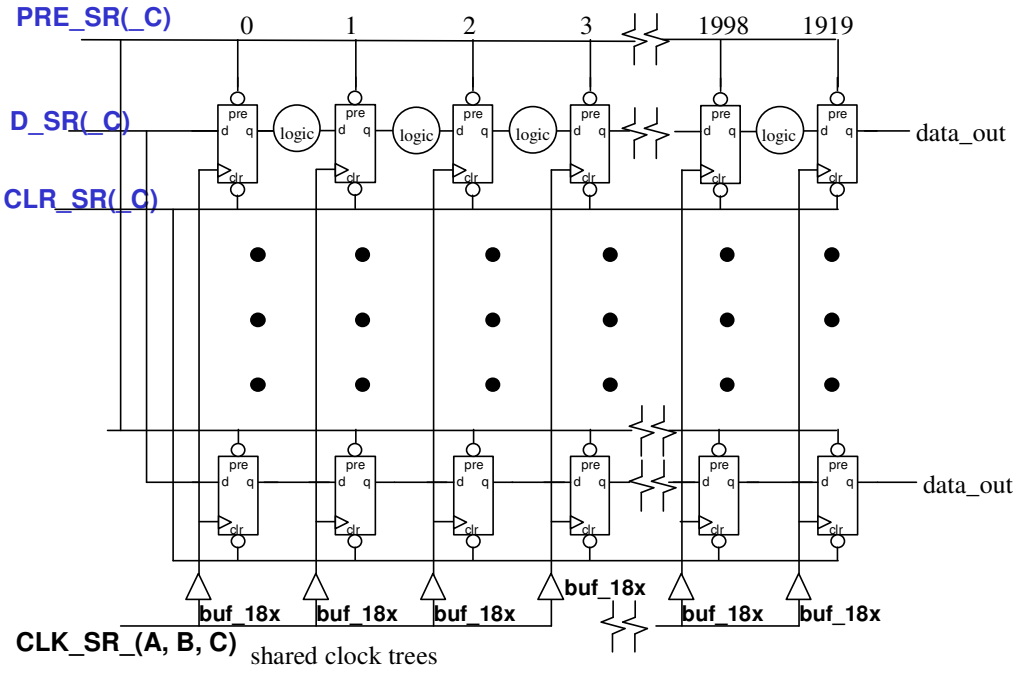
No errors were observed on any SR string with either all-1 or all-0 pattern to the highest tested LET of 28.44.

Appendix 1: Detailed Shift Register Descriptions

TOP LEVEL - SHIFT REGISTERS - BLOCKS A, B, and C

Chip: : Boeing/ VU	**GROUP: Shift Registers(A,B, C)**	Updated: 12/07/04
Blocks: A, B, C (see subsequent sheets for details)		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_A, CLK_SR_B, CLK_SR_C, D_SR, D_SR_C, CLR_SR, CLR_SR_C, PRE_SR, PRE_SR_C		
OUTPUT PADS (by name): see subsequent sheets		
Description: Various 1920 bit shift registers for SEU and dose rate upset testing. The clock tree is to be wired "perpendicular" to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

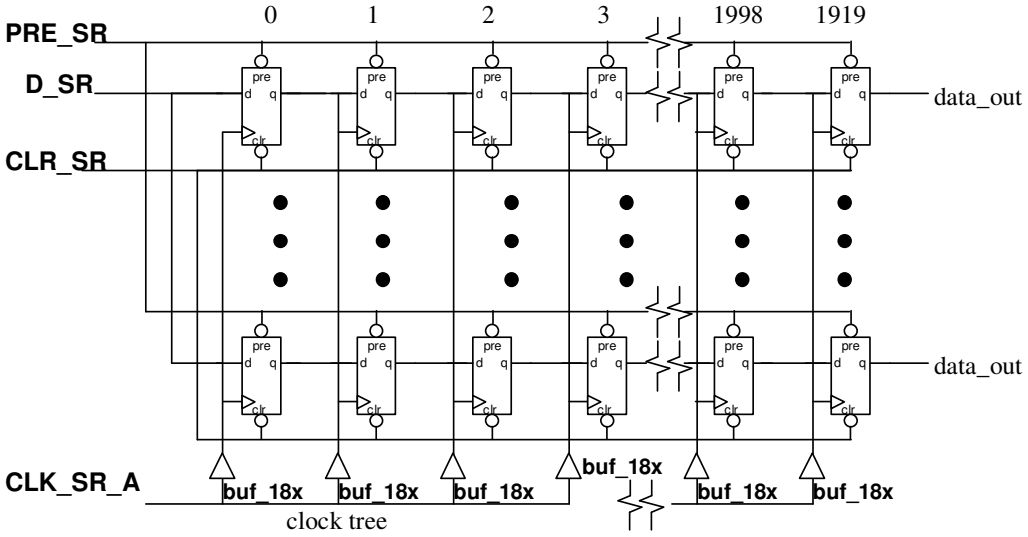
General Schematic



SHIFT REGISTERS – BLOCK A

Chip: : Boeing/ VU	Test Group: Shift Registers	Updated: 12/07/04
Block: Shift Register Block A		
Subcircuits: SR_DFF_CPQ_soft, SR_DFF_CPQ_hard, SR_DICE_soft, SR_DICE_soft_wide, SR_DICE_mdm, SR_DICE_hard		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_A, D_SR, CLR_SR, PRE_SR		
OUTPUT PADS (by name): see table below		
Description: Six 1920 bit shift registers for SEU and dose rate upset testing. The clock tree is to be wired "perpendicular" to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

General Schematic

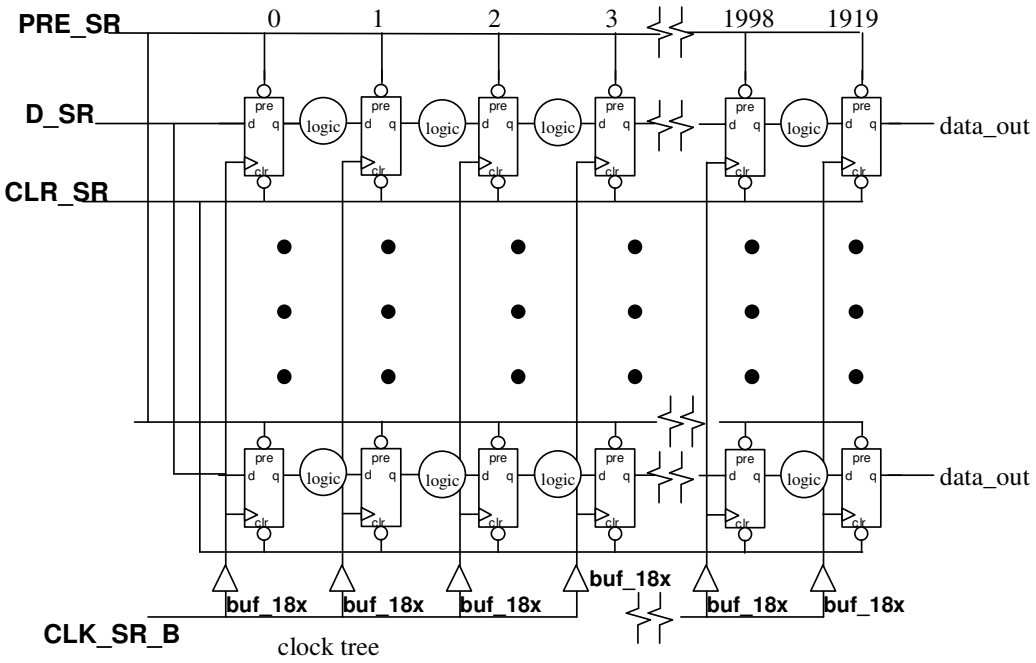


Circuit	FLIP/FLOP cell	OUTPUT
SR_DFF_CPQ_soft	dff_cpq	**OUT_ DFF_CPQ_soft**
SR_DFF_CPQ_hard	dff_cpq_annb	**OUT_ DFF_CPQ_hard**
SR_DICE_soft	dice_cpq	**OUT_ DICE_soft**
SR_DICE_soft_wide	dice_cpq_wide	**OUT_ DICE_soft_wide**
SR_DICE_mdm	dice_cpq_dbwt	**OUT_ DICE_mdm**
SR_DICE_hard	dice_cpq_annb	**OUT_ DICE_hard**

SHIFT REGISTERS – BLOCK B

Chip: : Boeing/ VU	Group: Shift Registers	Updated: 12/07/04
Block: Shift Registers B Subcircuits: see subsequent sheets		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_B, D_SR, CLR_SR, PRE_SR		
OUTPUT PADS (by name): see subsequent sheets		
Description: Four 1920 bit shift registers for SEU and dose rate upset testing. The clock tree is to be wired "perpendicular" to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

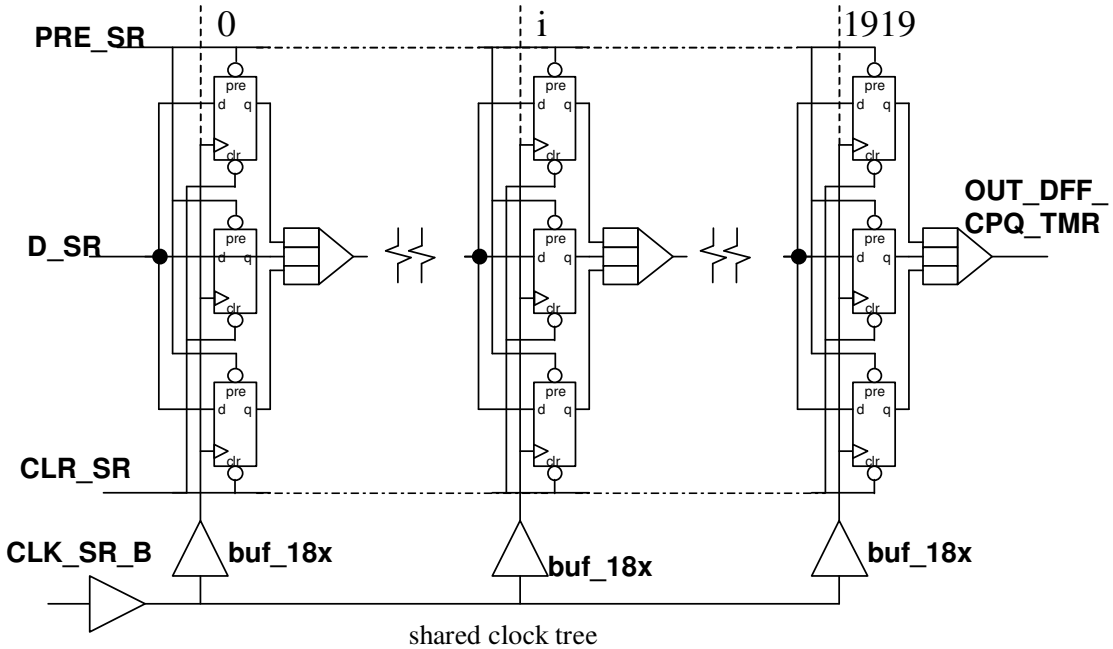
General Schematic



SHIFT REGISTERS – BLOCK B, Subcircuit - SR_DFF_CPQ_tmr

Chip: : Boeing/ VU	Test Group: Shift Registers	Updated: 12/08/04
Block: Shift Registers Block **B**		
Subcircuit Name: SR_DFF_CPQ_tmr		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_B, D_SR, CLR_SR, PRE_SR		
OUTPUT PADS (by name): OUT_DFF_CPQ_TMR		
Description: 1920 bit triple mode redundant soft shift register for SEU and dose rate upset testing. The clock tree is to be wired "perpendicular" to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

Schematic (preliminary)

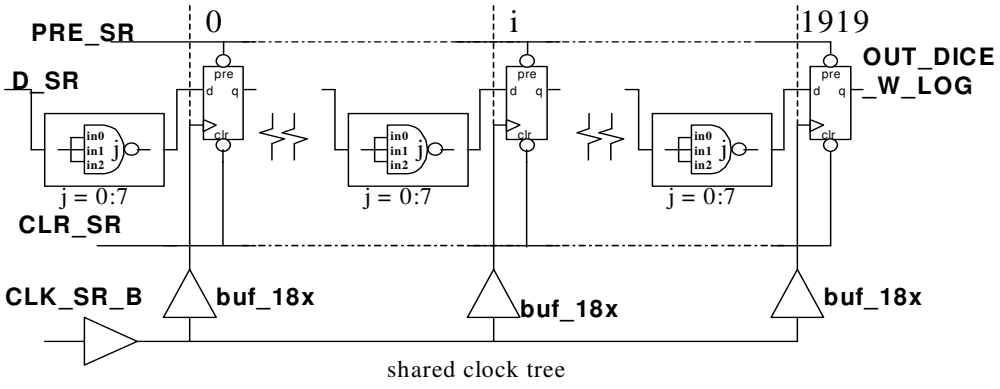


shared clock tree

SHIFT REGISTERS – BLOCK B, Subcircuit - SR_DICE_w_logic

Chip: : Boeing/ VU	Test Group: Shift Registers	Updated: 12/08/04
Block: Shift Register Block **B**		
Subcircuit Name: SR_DICE_w_logic		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_B, D_SR, CLR_SR, PRE_SR		
OUTPUT PADS (by name): OUT_DICE_W_LOG		
Description: DICE FLIP/FLOPs with intervening combinational logic shift register for SEU and dose rate upset testing. All cells in this shift register are from the soft library. This SR is to be tested at maximum attainable clock rate to investigate clock dependent effects. The clock tree is to be wired "perpendicular" to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

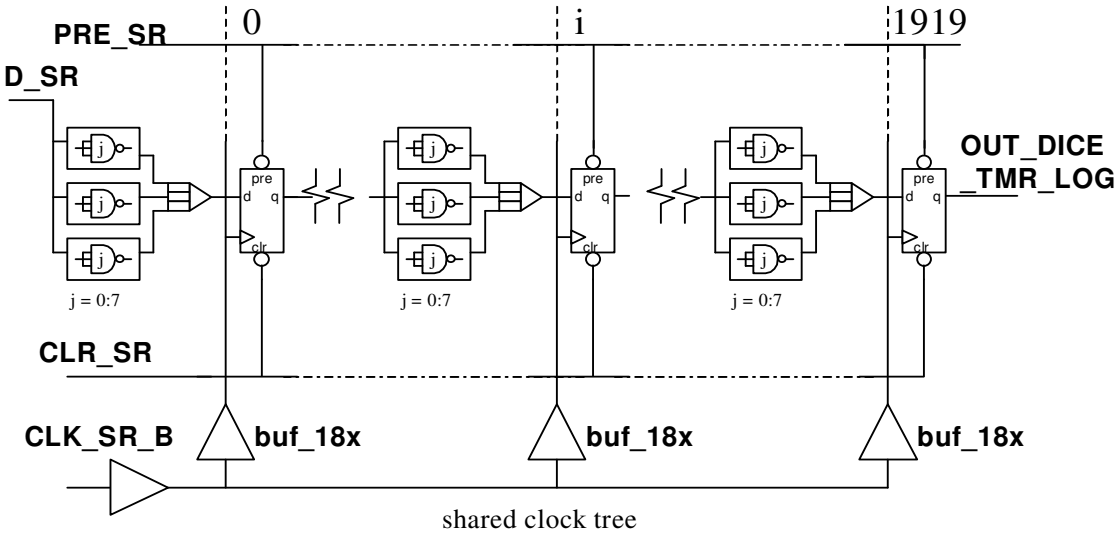
Schematic (preliminary)



SHIFT REGISTERS – BLOCK B, Subcircuit - SR_DICE_TMR_LOG

Chip: : Boeing/ VU	Test Group: Shift Registers	Updated: 12/08/04
Block: Shift Registers B		
Subcircuit Name: SR_DICE_TMR_LOG		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_B, D_SR, CLR_SR, PRE_SR		
OUTPUT PADS (by name): OUT_DICE_TMR_LOG		
Description: DICE FLIP/FLOPs with intervening TMR combinational logic shift register for SEU and dose rate upset testing. All cells in this shift register are from the soft library. This SR is to be tested at maximum attainable clock rate to investigate clock dependent effects. The clock tree is to be wired "perpendicular" to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

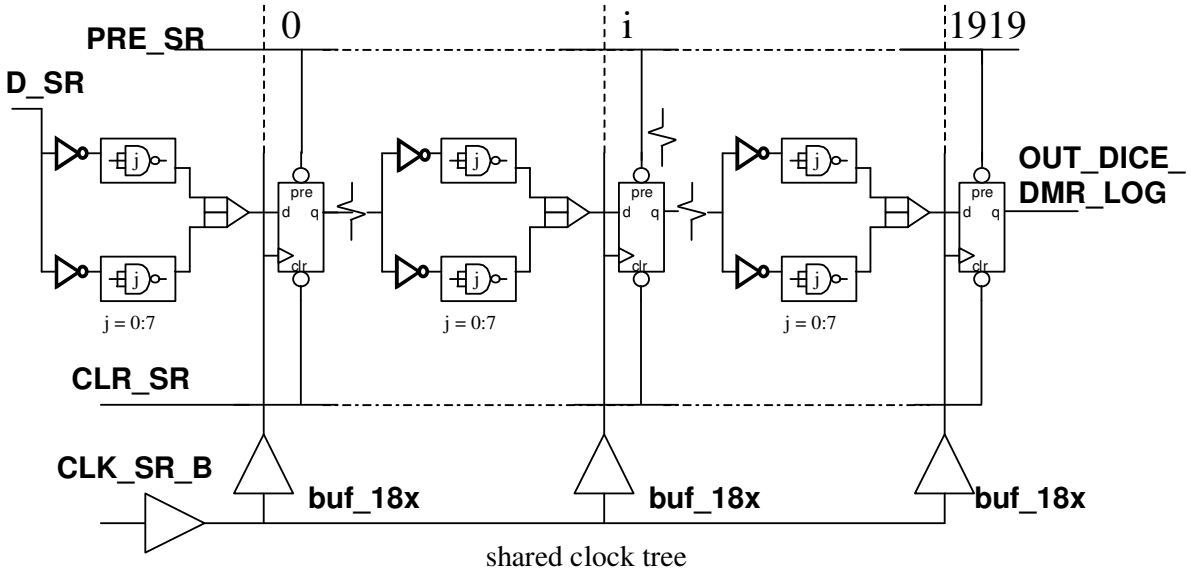
Schematic (preliminary)



SHIFT REGISTERS – BLOCK B, Subcircuit - SR_DICE_DMR_LOG

Chip: : Boeing/ VU	Test Group: Shift Registers	Updated: 12/08/04
Block: Shift Registers B		
Subcircuit Name: SR_DICE_DMR_LOG		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_B, D_SR, CLR_SR, PRE_SR		
OUTPUT PADS (by name): OUT_DICE_DMR_LOG		
Description: DICE FLIP/FLOPs with intervening DMR combinational logic shift register for SEU and dose rate upset testing. All cells in this shift register are from the soft library. This SR is to be tested at maximum attainable clock rate to investigate clock dependent effects. The clock tree is to be wired “perpendicular” to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

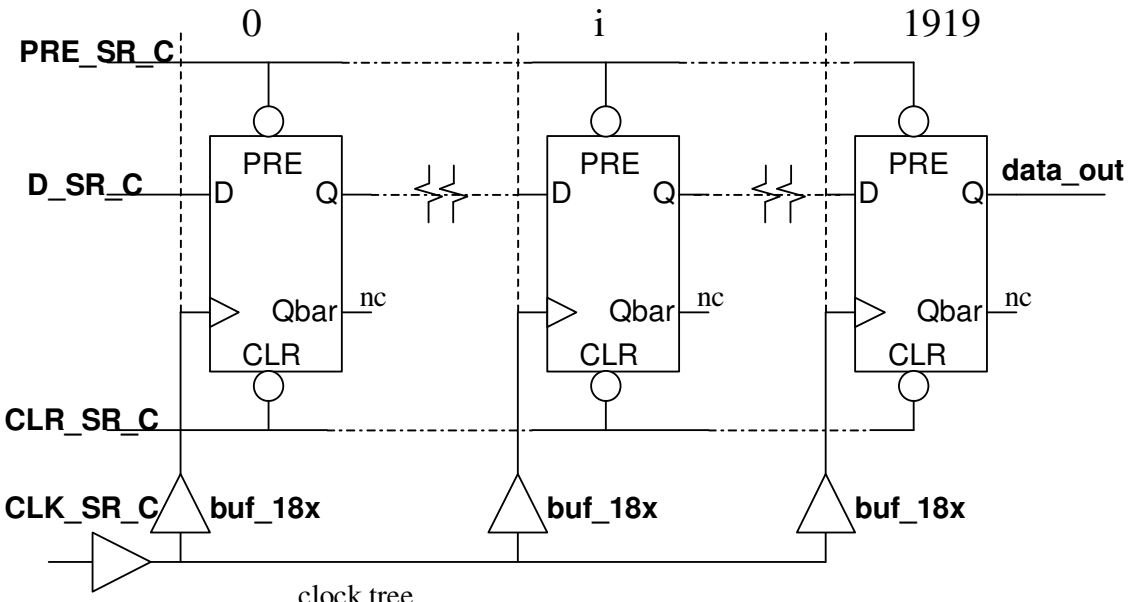
Schematic (preliminary)



SHIFT REGISTERS – BLOCK C

Chip: : Boeing/ VU	Test Group: Shift Registers	Updated: 12/22/04
Block: Shift Registers C		
Rad Tests: SEE (heavy ion, laser, microbeam), Dose Rate		
SUPPLY PADS (by name): VDD_CORE_SR, VSS_CORE_SR, VDD_PADS_SR, VSS_PADS_SR. Global		
INPUT PADS (by name): CLK_SR_C, D_SR_C, CLR_SR_C, PRE_SR_C		
OUTPUT PADS (by name): see table below		
Description: 7 1920 bit shift registers for SEU and dose rate upset testing. The clock tree is to be wired "perpendicular" to the register strings such that upsets due to clock branch hits may be distinguished from register hits.		

Schematic (preliminary)



Circuit	FLIP/FLOP cell	OUTPUT
SR_DICE_ISDE	dice_latch_final	**OUT_ DICE_ISDE**
SR_GG2_ISDE	gg2_latch_final	**OUT_ GG2_ISDE**
SR_GG_ISDE	gg_latch_final	**OUT_ GG_ISDE**
SR_DYNTMR_ISDE	dynamic_tmr_final	**OUT_ DYNTMR_ISDE**
SR_DICEGN_ISDE	dffdice_cpqgn_final	**OUT_ DICEGN_ISDE**
SR_DICEOW_ISDE	dffdice_cpqow_final	**OUT_ DICEOW_ISDE**
SR_DICESW_ISDE	dffdice_cpqsw_final	**OUT_ DICESW_ISDE**